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PTMAC BASED ON RAZOR FOR ENERGY REDUCTION IN DSP

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Abstract

The power optimization is achievable by dynamic voltage scaling using the fault tolerant technique by improving the accuracy and/or timing performance against power. Energy improvements have a strong dependency on the delay distribution of the circuit and the characteristics of the input signal. The fault tolerant technique is implemented using Razor approach. The target power is also obtained by using the programmable truncated multiplier (PTMAC) at the expense of degradation of the output signal to noise ratio. In the DSP architecture, the combination of PTMAC and fault tolerant technique is used to reduce the supply voltage below the critical level. Truncated multiplication timing modulation properties are analysed and demonstrated using Xilinx 12.1. Finally the two techniques upgrade the energy saving beyond that expected in the DSP architecture.

Key words: PTMAC, DSP, Razor, energy reduction.

INTRODUCTION

Less power, area with high speed is the main theme in the VLSI based circuit design. Several techniques exist to reduce the energy consumption.

Voltage scaling is an effective technique to reduce the energy consumption in CMOS integrated circuits. The (DSP) digital signal processing system may possibly leverage unconventional voltage overscaling (VOS) to reduce energy consumption while maintaining satisfactory signal processing performance. Scaling the supply

voltage by a factor of K results in reduction in the dominating dynamic power consumption by a factor of K^2 and yields static power benefits [1].

In conventional practice, voltage scaling is lower bounded by $V_{dd\text{-}crit}$ (critical supply voltage) under which critical path delay equals the target clock period, voltage overscaling (VOS) (i.e.), overscaling the supply voltage below $V_{dd\text{-}crit}$. Digital signal processing systems by applying unconventional voltage overscaling levels to further improve the energy consumption levels while maintaining signal processing performance. The major disadvantage of VOS is the latches or flip-flop on the critical path need a long execution time [3]-[5].

Fault tolerant is a property that enables a system to continue operating properly in the event of failure. This technique can be used to achieve power saving. It is dependent on process voltage temperature (PVT) and the circuit physical design.

The ultimate aim is to design a multiplier of which possess less area usage and power that is possible with the truncated multiplier [6]-[12]. The PTM describes a full precision multiplier in which the elements of the partial product can be disabled a column wise manner through an external control word. This provides reduction in the dynamic power consumption. The advantages include dynamic power reduction and Flexibility in accuracy selection.

Manuel de la Guia Solaz and Richard Conway proposed a novel voltage management technique for dynamic voltage scaled (DVS) processor, based on it situ error detection and correction, called Razor [4]. In this technique, we use a delay-error tolerant flip-flop on the critical path to scale the supply voltage.

The PTMAC and the fault tolerant techniques are applied to a custom-designed fixed point multiply and accumulate (MAC) in the DSP structure.

The rest of this paper is organised as follows. The voltage scaling, fault tolerant and truncated multiplication concept is dealt with in section II. Section III briefly explains the programmable truncated multiply and accumulate (PTMAC) architecture. The combination of the PTMAC and the fault tolerance using Razor technique is analysed in section IV. Simulation result for power and energy reductions is reported in section V. Finally in section VI conclusion and scope for future work on this paper are presented.

II BACKGROUND

A. Voltage Scaling Beyond $V_{dd\text{-}crit}$

Dynamic power consumption is the dominating component in many arithmetic unit circuits because of the high toggling profile of such structures. The switching component of the energy consumed by a digital gate is defined as $P\text{avg} = \alpha 0 \rightarrow 1 CLV2$ dd $f$clk in [13], where $\alpha 0 \rightarrow 1$ is defined as the average number of times in each clock cycle (at a frequency $f$clk) that a node with capacitance CL makes a power consuming transition. Reducing the supply voltage by a factor of K results in a quadratic improvement in the power consumption rate of CMOS logic.

Scaling of Vdd results in timing penalties which increase as Vdd approaches the threshold voltages of the devices [14]. Relationship between the circuit delay (τd) and the supply voltage Vdd is given by $\tau d = CLV\text{dd}/\beta(V\text{dd} - Vt\ )\alpha$, where CL is the load capacitance, β is the gate transconductance, Vt is the device threshold voltage, and α is the velocity saturation index. We refer to the critical supply voltage of a given architecture Vdd−crit, as the minimum supply voltage where timing on the critical path is met for any expected PVT variations.

Scaling the supply voltage to $V\text{dd} = K \cdot V\text{dd}-\text{crit}$, where $0 < K < 1$ is referred to as VOS; although this technique results in further energy reductions almost proportional to $K2$, scaling Vdd below the critical supply voltage results in critical

timing failures for certain input combinations under certain PVT conditions. This is impractical for use with designs that do not apply fault tolerant schemes.

III TRUNCATED MULTIPLICATION

Multipliers have become inevitable with the advancement of communication. In order to enable the implementation of complex algorithms in DSP architectures the advancing VLSI play a significant role. A truncated multiplier is an n × n multiplier with n bits output. Since in a truncated multiplier the n less significant bits of the full-width product are discarded, some of the partial products are removed and replaced by a suitable compensation function, to trade- off accuracy with hardware cost. As more columns are eliminated, the area and power consumption of the arithmetic unit are significantly reduced, and in many cases the delay also decreases. Truncated Multiplier has the advantage of reducing power consumption in the DSP systems. It is most commonly used in systems where least significant part of partial product can be skipped or disabled which leads to low power consumption, area and timing. Here the partial product is split into two sections namely the Least Significant Part (LSP) and Most Significant Part (MSP). The LSP is disabled or avoided to get the truncated output.

Truncated multiplication has been widely studied as a means of achieving both power and area improvements in the field of arithmetic circuit design, at the expense of signal degradation. As the truncated multipliers are smaller than full-precision ones, they not only achieve improvements in power consumption and area, but result in different timing distributions. The existence of synergic benefits derived from the combination of truncated multiplication and VOS using a fault tolerance strategy is presented in this brief where both techniques are applied to a custom-designed fixed point multiply and accumulate (MAC) structure.

IV PTMAC-A FLEXIBLE LOW-POWER DSP WITH PTM

To extend the usage of PTM to general DSP architectures, the PTMAC was introduced and analyzed in [12] and [19]. PTMAC, designed as a vehicle to exercise PTM in low-power biomedical applications with a need for modest DSP such as ECG filtering or fall detection, will be utilized in this brief as a platform to combine the benefits of programmable truncation and fault tolerance.

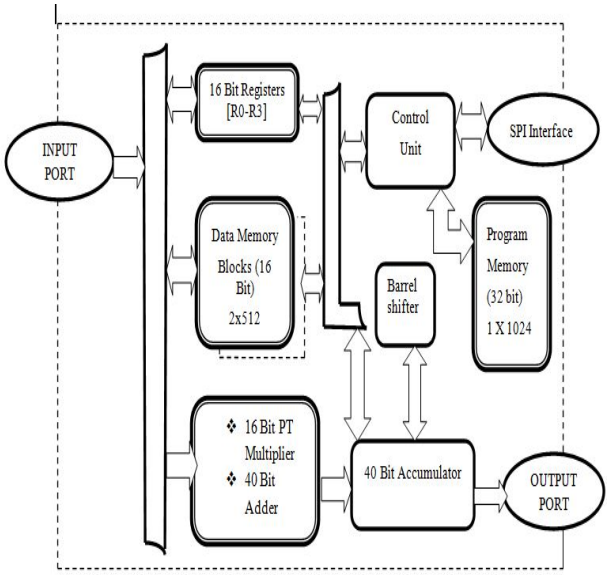

Fig.1. PTMAC top level diagram.

The proposed DSP, as depicted in Fig. 1, includes a control unit operating in a five-stage pipeline, program and memory blocks in a multibus Harvard configuration, some I/O connectivity and an arithmetic unit consisting of a MAC structure with a 16-bit PTM, a 40-bit accumulator, and a 40-bit barrel shifter for scaling and rotating the accumulated value.

The following gives the description of the main components of the DSP architecture.

1) Control unit: The control unit is a simple 5 stage pipeline which fetches and decodes the instruction also controls the data flow ,controls the ALU operations. The main aim of the design of the control unit is to reduce the power consumption of the internal blocks other than the arithmetic block. it allows the access of two data memory blocks and the program memory block during the instruction read operation.

2) Custom Instruction Set: A custom instruction set is implemented for the DSP so as to maximize the utilization of the ALU. This will help in optimizing the power reductions Offered by the programmable truncated multiplier. All the Instructions designed are 32 bits wide. The set of instructions include

- **Arithmetic and logic instructions:** The arithmetic instruction include addition operation, subtraction, multiplication with and without truncation and also other operations such as multiply and accumulate operation, shifting and rotation of the accumulator output also squaring of the accumulated value. All the arithmetic instructions utilize the arithmetic unit effectively. A logic instruction performs all the logic operations.
- **Flow control instructions:** The flow control instructions include instructions for jump operation, loop operations. Table III presents a list of such instructions.
- **Dataflow instructions:** It includes instructions for storing and loading data to and from different memory blocks.

3) Memory blocks: The memory blocks include two data memory blocks a program memory block. Each data memory is of size 512 x16 bits and the program memory is of size 1024x32 bit. The data memory is used to store and load data, .and program memory is used to store the instructions. it is possible to access all the three memory blocks in a single clock cycle.

4) Arithmetic and logic unit: The ALU contains the 16 bit programmable truncated multiplier, a 40 bit carry select adder a 40 bit barrel shifter/rotator and a 40 bit accumulator. The ALU has a multiply and accumulate structure. . A block diagram of the Arithmetic Unit is displayed in Fig. The arithmetic unit consists of

- **PTM:** The PTM is designed to operate as a standard 16x16 bit multiplier that enables a programmable truncation. For that it includes an extra control input for enabling and disabling the columns in the partial product matrix. Thus the

extra control input “truncation control” is used to control the truncation level of the multiplier.

- **Barrel shifter:** A 40 bit barrel shifter/rotator is used for shifting as well as rotating the accumulated output. The shifter performs left shifting, left rotation, right shifting and right rotation on the 40 bit accumulator output.

- **Accumulator:** A 40 -bit accumulator stores the final result of the arithmetic operations. It is constructed from D flipflops.

- **Carry Select Adder:** A 40- bit carry select adder is used for addition as well as subtraction operations. The carry select adder is a simple but high speed adder. The logic unit performs all logic operations on the two input data.

V RAZOR IMPLEMENTATION

To achieve the fault tolerance, the accumulator unit of the PTMAC was replaced by a fault tolerant version named Razor Accumulator where the original flip-flops were substituted by a version of the Razor registers presented in [3] and [20].

In order to detect an error at the circuit level, each flip-flop is augmented by a shadow flip-flop which is clocked by a delayed clock. If the combinational logic met the setup time of the main flip-flop, then the main and delayed flip-flop will latch the same value. In this case, the error signal remains low. If the setup time of the main flip-flop is not met, then the main flip-flop will latch a value that is different from the shadow flip-flop.

The proposed augmented cells were designed and stored as library cells for post synthesis insertion. Such a cell follows the original implementation Razor implementation, replacing the shadow latch within the Razor registers with a shadow-flip-flop to avoid synthesis issues. The metastability detector required in Razor implementations was modelled as the delay of an inverter added as a constraint to the hold time of the Razor accumulator. In this way, all timing violations potentially

causing metastability are then detected as timing errors, providing a lower bound for the performance of Razor.

The Razor technique was implemented using NI multisim suite 12.0 software.

VI RESULTS

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	0	46560	0.0
Signals	0.000	178	---	---
IOs	0.000	66	240	27.5
DSPs	0.000	2	288	0.7
Leakage	0.712			
Total	0.712			

Fig .2. Power value of normal multiplier

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	61	46560	0.1
Signals	0.000	109	---	---
IOs	0.000	67	240	27.9
Leakage	0.712			
Total	0.712			

Fig .3. Power value of PT Multiplier

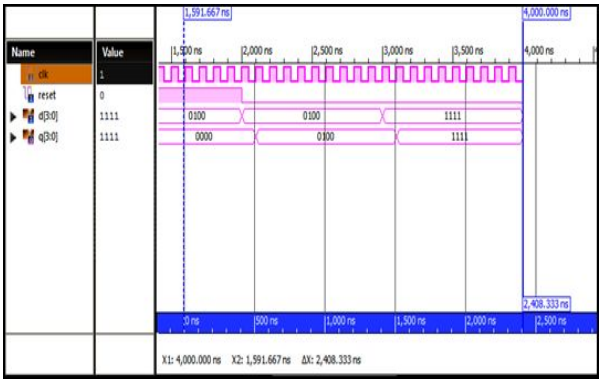

Fig .4. Simulation result of 16 bit Register

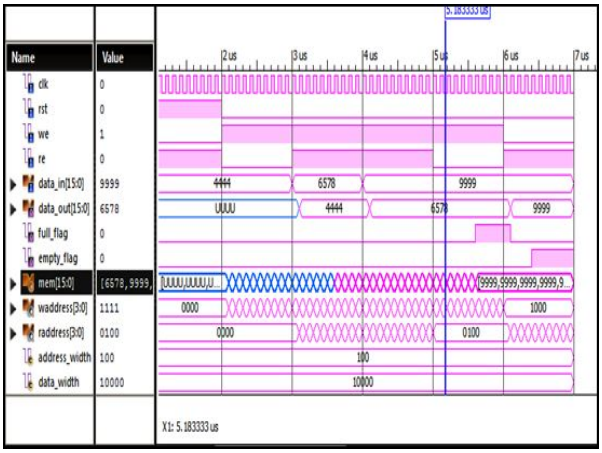

Fig .5. Simulation result of data memory

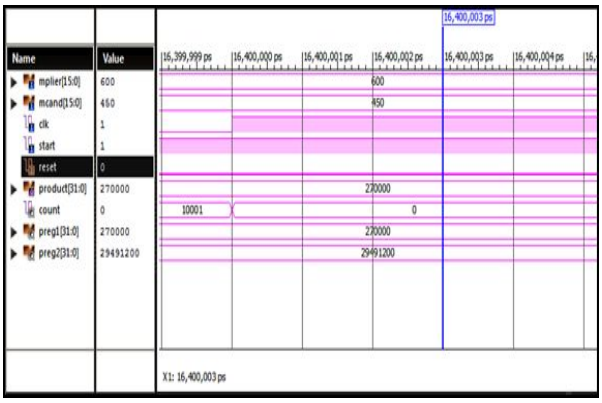

Fig .6. Simulation result of 16 bit PT multiplier

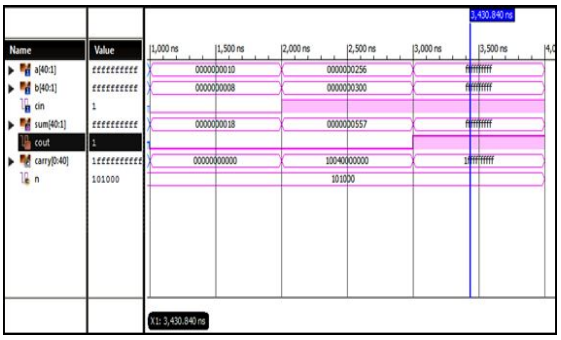

Fig .7. Simulation result of 40 bit Adder

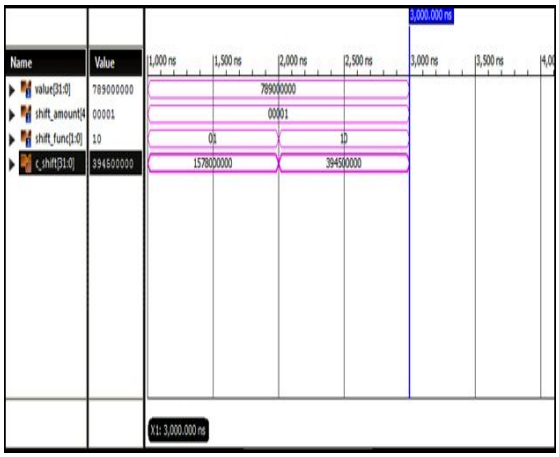

Fig .8. Simulation result of Barrel Shifter

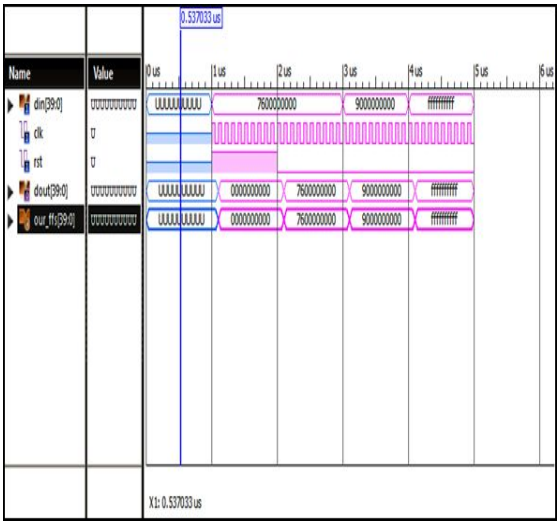

Fig .9. Simulation result of Accumulator

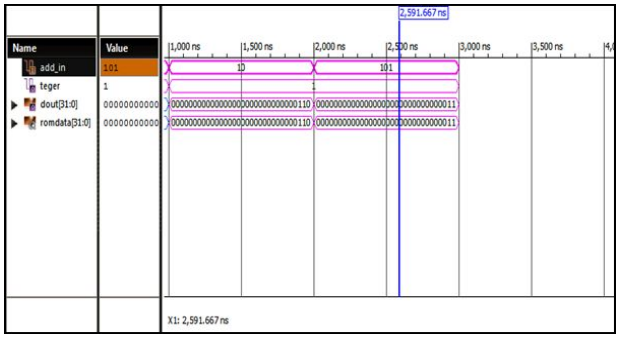

Fig .10. Simulation result of Program memory

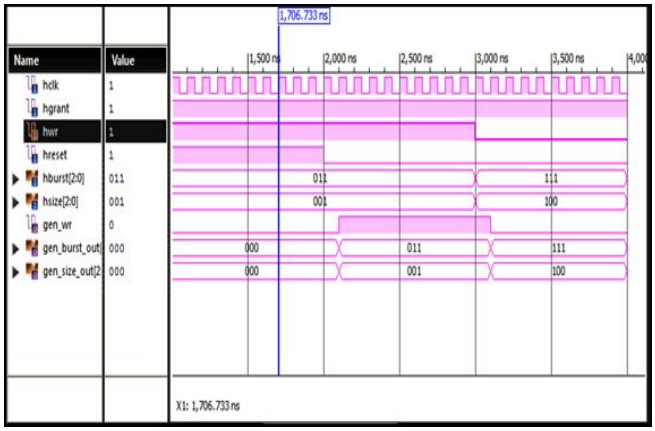

Fig .11. Simulation result of Control Unit

A. COMPARISION

MULTIPLIER	POWER (in %)
Normal Multiplier	28.2

SUPPLY VOLTAGE(V)	PTMAC BLOCK	RAZOR TECHNIQUE
20 V	800 (pW)	425 (pW)
17 V	578 (pW)	314 (pW)
12 V	288 (pW)	169 (pW)
10 V	200 (pW)	125 (pW)
7 V	98 (pW)	74 (pW)

Table .2. Overall power value

PT Multiplier	28.0

Table . 1. Power range of Normal and PT multiplier

TECHNIQUE	POWER (in %)
PTMAC BLOCK	81.9
MODIFICATION IN SP INTERFACE	81.8

Table .3. Power of PT and Razor technique

VII CONCLUSION

Fault tolerance was provided by implementing a conservative approach to the Razor I technique, and achieved energy reductions over the original DSP implementation by enabling the reduction of V_{dd} beyond the original critical supply level. Truncated multiplication was achieved by implementing a PTM, and resulted in energy savings of the full design. Energy reductions achieved by fault tolerant techniques are limited by the overheads required to provide error resilience and the amount of operations that need correction, therefore, they are highly influenced by the delay distribution and maximum value of the system critical paths. The truncated multiplication is achieved by interfacing them effectively with respect to the conditions after checking and monitoring than the previous method. The use of Razor on a PTMAC structure has been tested at a post synthesis simulation level to study the effect and interactions of both energy reducing techniques on a previously tested DSP design. The timing and power effects of VOS with error correction and the application of programmable truncated multiplication resulted in significant power reductions. The power consumption of Razor on a PTMAC structure is also implemented in Multisim software. Thus, we have analyzed and compared the performance results better than the conventional approach in terms of area, power and speed.

In the future work, delay-modulation properties of truncated multiplication and BIST using testable circuits can be exploited to improve the energy consumption of fault tolerant DSP architectures where multipliers are involved in the critical path of the circuit.

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